PSIET,KARANDA,DHENKANAL

LESSON PLAN

Session (2022-2023)

Discipline : ETC	Semester:4th,summer/2023	Name of the Teaching Faculty: Subhakanta Pradhan
Subject: Microprocessor and Microcontroller	No. of Days/Week Class Allotted -4	Semester From Date: 15.02.2023 To Date: 23 .05.2023 No. of Weeks: 15
Week	**Class Day**	**Theory Topics**
1st	1st	Discussion of microprocessor and its application
	2nd	Distinguish between microprocessor and microcomputer
	3rd	Discussion of Architecture of processor and Bus system in processor
	4th	Pin configuration of Intel 8085 microprocessor
	5th	Pin configuration of Intel 8085 microprocessor
2nd	1st	Architecture of Intel 8085 processor
	2nd	Revising the taught portions
	3rd	Doubt clearance
	4th	Pin configuration of Intel 8085 microprocessor
	5th	Revising the taught portions
3rd	1st	Architecture of Intel 8085 processor
	2nd	Registers of Intel 8085. Distinguish between SPR and GPR
	3rd	Stack, stack pointer and stack top
	4th	Addressing modes in Intel 8085

4th	1st	Types of instruction
	2nd	Simple programming examples
	3rd	Basic assembler Directives
	4th	Programming on logic operations
	5th	Basic assembler Directives
5th	1st	Programming on logic operations
	2nd	Programming on Delay
	3rd	**Quiz 1**
	4th	Programming on looping, counting , Indexing(JMP and CALL)
	5th	Programming on Delay
6th	1st	Compare between two numbers, Arrray Handling, code conversion
	2nd	T-state, Fetch cycle, Machine cycle and Instruction cycle
	3rd	T-state, Fetch cycle, Machine cycle and Instruction cycle
	4th	Differentiate between Instruction cycle, machine cycle and T state
	5th	Differentiate between Instruction cycle, machine cycle and T state
7th	1st	Timing diagram of MOV,DCR,MVI,LDA,DCX
	2nd	Timing diagram of MOV,DCR,MVI,LDA,DCX
	3rd	Timing diagram of MOV,DCR,MVI,LDA,DCX
	4th	Timing diagram of MOV,DCR,MVI,LDA,DCX
	5th	Timing diagram of MOV,DCR,MVI,LDA,DCX
8th	1st	Revision of Timing diagram Doubt clearance
	2nd	Pin configuration of Intel 8255 and discussion of interfacing
	3rd	Memory mapping and IO mapping
	4th	Memory interfacing with RAM and EPROM
	5th	Memory interfacing with RAM and EPROM

9th	1st	8257 DMA controller and 8259 programming interrupt controller
	2nd	Traffic light controlling, stepper motor control
	3rd	ADC and DAC interfacing
	4th	Internal architecture of Intel 8086, maximum and minimum mode
	5th	Revision
10th	1st	Internal architecture of Intel 8086, maximum and minimum mode
	2nd	Assignment
	3rd	Checking of assignment
	4th	Class test
	5th	Copy checking
11th	1st	Internal ready revision
	2nd	Pin details of 8086
	3rd	Pin details of 8086
	4th	Addressing modes of 8086
	5th	Addressing modes of 8086
12th	1st	Instruction set of 8086
	2nd	Instruction set of 8086
	3rd	Simple programming
	4th	**Quiz -2**
	5th	Evulation of Quiz
13th	1st	Distinguish between Microprocessor & Microcontroller
	2nd	8 bit & 16 bit microcontroller
	3rd	CISC & RISC processor
	4th	Architectureof8051Microcontroller
	5th	Architectureof8051Microcontroller
14th	1st	Signal Descriptionof8051Microcontrollers
	2nd	Memory Organisation-RAM structure, SFR
	3rd	Registers,timers,interruptsof8051Microcontrollers
	4th	Addressing modes of 8051
		Addressing modes of 8051
15th	1st	Simple 8051 Assembly Language Programming

		Arithmetic& Logic Instructions , JUMP, LOOP, CALL Instructions, I/O Port Programming
	2nd	Interrupts, Timer & Counters , Serial Communication
	3rd	Microcontroller interrupts and interfacing with 8255
	4th	Final revision, previous year questions discussion.
	5th	Final revision, previous year questions discussion.

Signature of the faculty

15/2/2023

Signature of the Principal